Distributed Fiber Optic Sensing: Measuring Temperature on a Printed Circuit Board

Contents

Introduction

A simple experiment was conducted to demonstrate how distributed temperature sensing with Luna's ODiSI-B can be used to identify a possible point of failure in an integrated electrical component system. In this test, a fiber optic temperature sensor was used to measure the temperature profile of a set of circuit boards. Temperature was measured across several electronic printed circuit boards with a single fiber optic temperature sensor.

Prior to testing, there was a known issue with the board. During normal operation, communication between the board and the host PC would break down. Repeated failures and further inquiry led to the conclusion that the board set was overheating due to poor internal airflow in the system in which it was installed.

Distributed temperature measurements with the ODiSI-B were used to create a temperature profile along the circuit board components. Looking at hotspots along the temperature profile allowed for identification of chipsets that exceeded their recommended operating temperature and were the cause of system failure. Knowing which components were causing system failure enabled re-work of the design to increase system reliability.

Test Setup

With the conclusion that poor airflow within the system was a problem, it became necessary to identify which components on the boards were exceeding their operating temperature. Once this was known, a solution could be engineered and corrective action could be taken. Since there was no internal monitoring of the chip temperatures other than the FPGA, an ODiSI-B system was used to measure temperature at

locations along the detector board, laser board and high voltage power supply. To minimize the effect of strain on the temperature measurements, the sensing fiber was routed through Teflon tubing that was attached to the surfaces of the heat sinks or the chips themselves with ¼" Kapton tape discs. The Teflon tubing prevents strain from coupling in to the temperature measurement by allowing the sensor to float freely inside the tube. The tubing allows the sensor to be taped to the points of interest while still floating so that any changes it experiences will be due to heating or cooling and not mechanical strain.

The ODiSI-B was configured for high-resolution measurements (1.25 mm gauge length and sensor spacing at 23.8 Hz for sensors up to 10m). The reference scan was taken when the board was powered down to provide a temperature baseline. In order induce a quicker failure event, the system with the circuit board was fully enclosed and placed close to a wall to limit the amount of airflow over the circuitry. The system was then monitored for failures.

The gold-colored sensing fiber path can be seen in Figures 1 and 2 below. The high voltage power supply is not visible in either of these figures. To have a secondary and repeatable set of data, the single sensing fiber was looped back and crossed twice over the chipsets of interest.

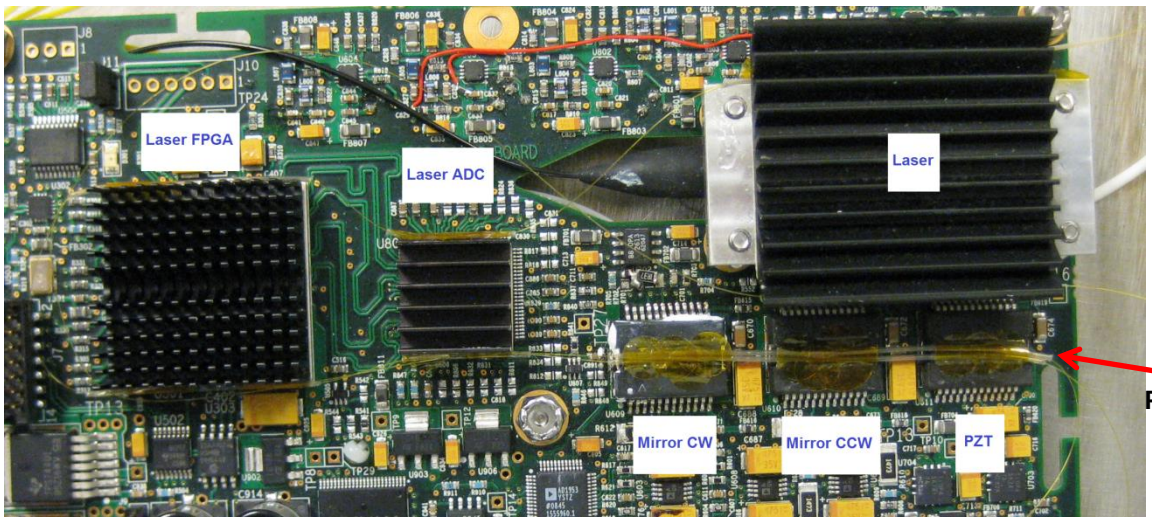

Figure 1. Sensing fiber positioned on laser board. The fiber is routed through Teflon tubing attached to the laser, the laser ADC, the laser FPGA, and three op-amps. Note that the fiber passes twice across each chip.

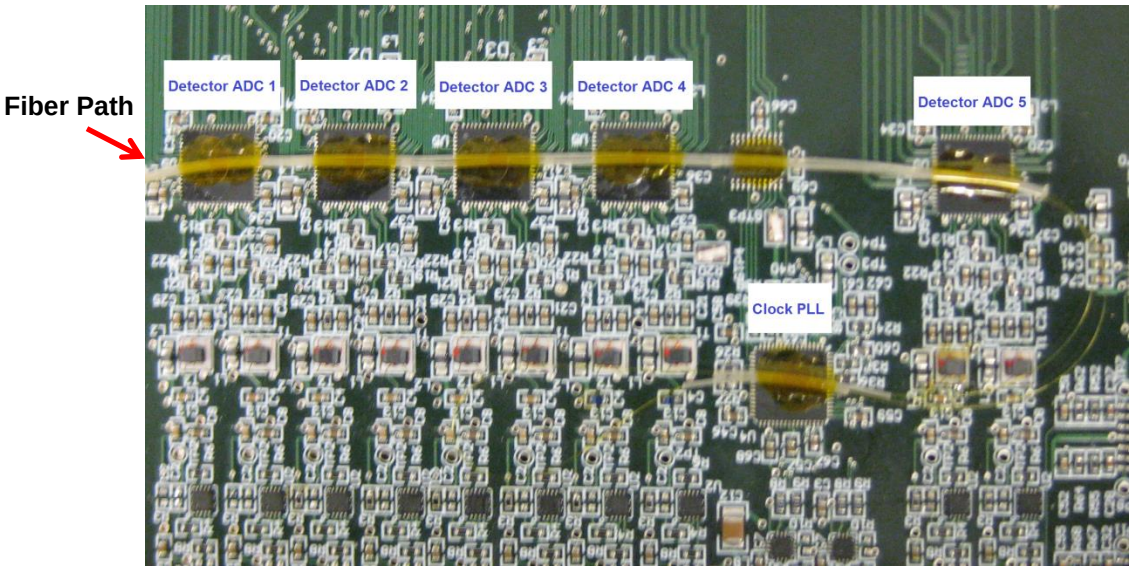

Figure 2. Sensing fiber positioned on the detector board. The fiber is routed through Teflon tubing attached to 5 ADCs, a level translator, and a clock PLL. Note that the fiber passes twice across each chip.

Results and Discussion

Prior to conducting the test, it was necessary to map the physical components of interest with respect to distance along the fiber path. This was done by the Touch-to-Locate[1] method where a controlled localized temperature change is induced at the point of interest, which is manifested as a temperature peak in the ODiSI-B GUI. The position of that peak is recorded and repeated for any other physical points of interest. The resulting locations are shown in Table 1 below.

Part / Integrated Circuit of Interest	Sensing Fiber Location Pass 1 (mm)	Sensing Fiber Location Pass 2 (mm)
Laser	0.541 - 0.605	2.308 – 2.357
Laser ADC	0.627 - 0.653	2.111 – 2.132
Laser FPGA	0.653 - 0.703	2.141 – 2.176
Laser Mirror CW	0.818 - 0.840	2.083 – 2.101
Laser Mirror CCW	0.840 - 0.862	2.062 – 2.083
Laser PZT	0.862 - 0.886	2.039 – 2.062
High Voltage Power Supply	1.039 – 1.095	1.817 – 1.878
Detector ADC 1	1.245 – 1.273	1.713 – 1.734
Detector ADC 2	1.273 – 1.288	1.696 – 1.713
Detector ADC 3	1.288 – 1.307	1.679 – 1.696
Detector ADC 4	1.307 – 1.324	1.662 – 1.679
Detector ADC 5	1.346 – 1.371	1.612 – 1.636
Clock PLL	1.415 – 1.436	1.516 – 1.537

Table 1. Location of each part of interest along sensing fiber.

Figure 3 shows an annotated temperature plot of a single pass of the fiber path. A communication failure occurred after 40 minutes. The system was allowed to run for an additional 5 minutes before shutdown. When looking at temperature versus time for each chip, we learn that after the failure event, all chips on the detector board begin cooling off, while all chips on the laser board continue to rise.

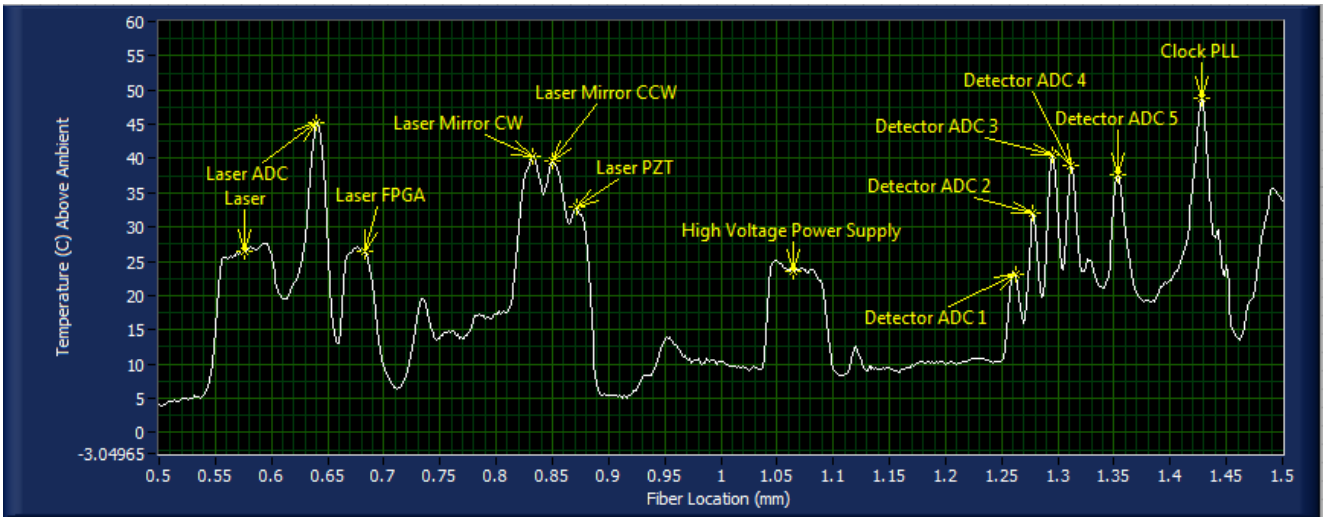

Figure 1. Temperature plot (degrees C above ambient) of the first 1.5 m of sensing fiber. The peaks correspond to the components of interest and are labeled accordingly.

The warmest chip is the Clock PLL, which at the time of failure was 52 °C above ambient temperature. This chip has no heat sink and is located in an area with limited airflow. An appropriate comparison chip would be the detector ADC 5 which also contains no heat sink and is located close to the Clock PLL. Temperature on detector ADC 5 at the time of failure read 42 °C above ambient. In normal operation, the Clock PLL dissipates 1.5W and the ADCs dissipate 1.25W. For these chips, the ratio of power dissipation (0.833) is approximately equal to their temperature ratios (0.808). Time-temperature plots of the Clock PLL and detector ADC 5 are shown in Figures 4 and 5 below.

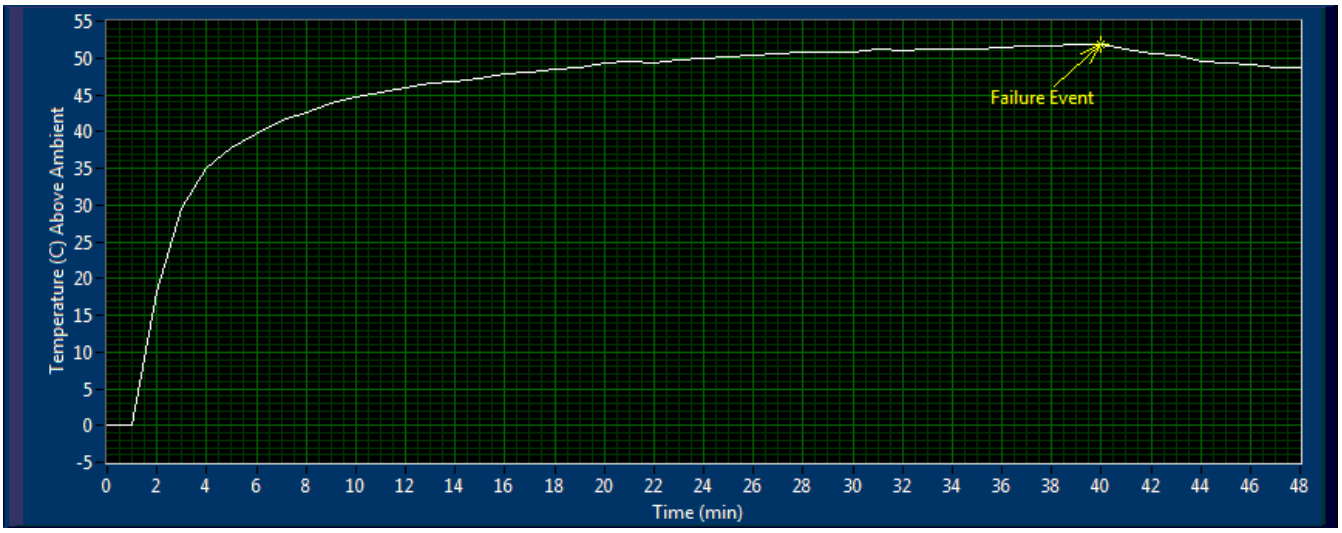

Figure 2. Time-lapse temperature plot of the Clock PLL. System failure occurs after 40 minutes.

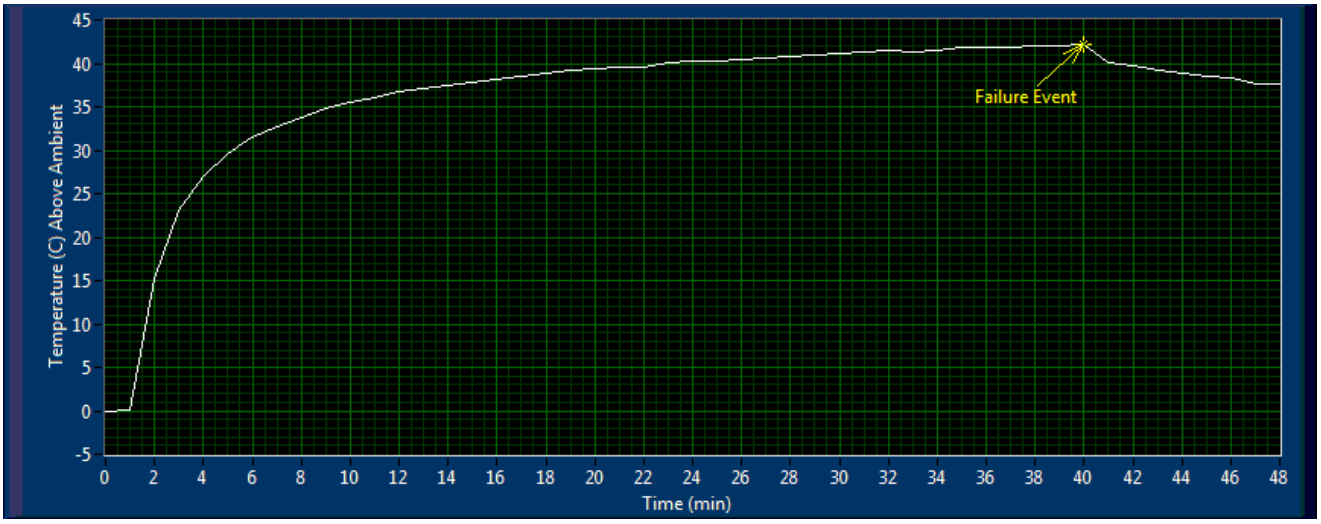

Figure 3. Time-lapse temperature plot of detector ADC 5. Again, system failure can be seen here after 40 minutes.

Power dissipation of the Laser ADC (approximately 1.61W at 50MHz) is greater than both the Clock PLL and detector ADC, but this is counteracted with a heat sink. Figure 6 shows the temperature versus time plot for the laser ADC. The temperature continues to rise after system failure, which suggests there is no failure in the laser board.

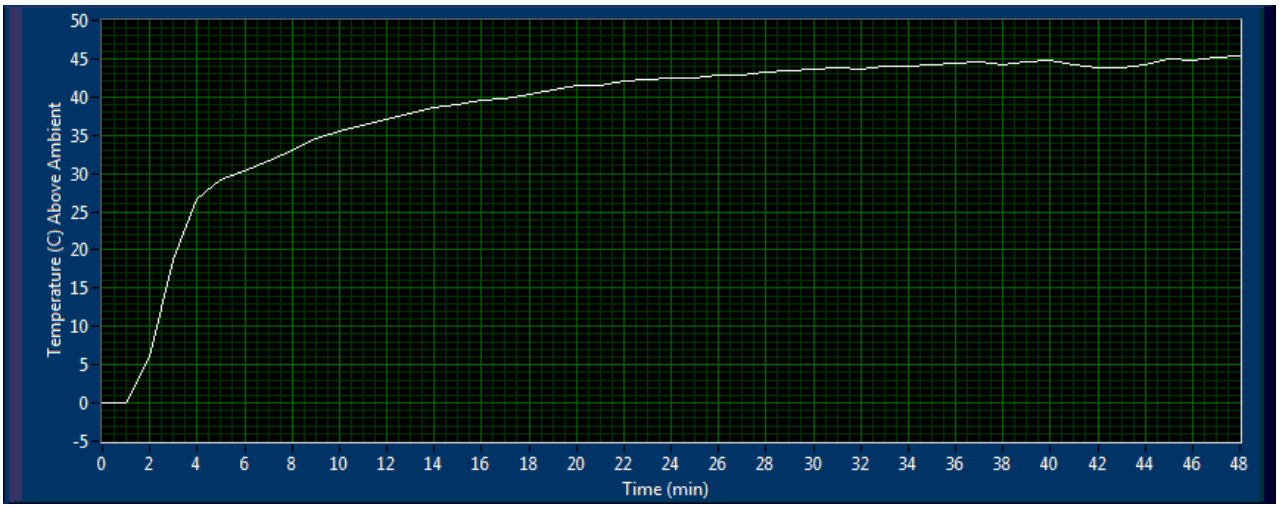

Figure 4. Time-lapse temperature of plot of laser ADC. The temperature continues to rise even after system failure occurs after 40 minutes.

The distributed temperature data shown earlier in Figure 3 was used to identify the point of failure along the detector board inside the system. These results allowed more accurate identification of which components were causing the issues. Design options were identified as potential solutions to cool the detector ADCs and Clock PLL.

Conclusion

Distributed temperature data provided by the ODiSI-B system enabled identification of overheating electrical components in an integrated circuit board set. Utilizing the full temperature profile of the circuit boards gave the ability to isolate points of failure and created possibilities for more cost effective solutions to the larger problem.

1. Touch to Locate Video Demonstration: http://www.youtube.com/watch?v=Tz1I3om9NGA

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